

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	Attorney Docket No. AUS920030226US1
Wendy Ann Belluomini, et al.	§	
	§	
Serial No. Not yet assigned	§	Examiner: Not yet assigned
	§	
Filed: Herewith	§	
	§	
For: Method and Apparatus for Low	§	Group Art Unit: Not yet assigned
Overhead Circuit Scan	§	

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97(b)


Mail Stop Patent Application
 Commissioner for Patents
 PO Box 1450
 Alexandria, Virginia 22313-1450

Sir:

Applicants submit the following information on (Substitute) Form PTO-1449 listing references pursuant to 37 CFR 1.97(b). Copies of the references listed on (Substitute) Form PTO-1449 are included herewith.

No fee is believed to be necessary; however, in the event that any fee is required, please charge it to **IBM Deposit Account Number 09-0447**.

Respectfully submitted,



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Substitute form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known		
				Application Number	Not yet assigned	
				Filing Date	Herewith	
				First Named Inventor	Wendy Ann Belluomini, et al.	
				Group Art Unit	Not yet assigned	
				Examiner Name	Not yet assigned	
Sheet	1	of	1	Attorney Docket Number	AUS920030226US1	
U.S. PATENT DOCUMENTS						
Examiner Initials	IDS Doc #	U.S. Patent Document Number	Name of Patentee or Applicant		Publication Date MM-DD-YYYY	
FOREIGN PATENT DOCUMENTS						
Examiner Initials	IDS Doc #	Office	Foreign Patent Document No.	Name of Patentee or Applicant	Date of Publication	English Translation
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS						
Examiner Initials	IDS Doc #	Include the name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			English Translation	
	A1	HANS JACOBSON, ET AL., <i>Synchronous Interlocked Pipelined CMOS</i> , IBM Corporation, pp. 1-12				
	A2	ERIC MERCER, ET AL., <i>Stochastic Cycle Period Analysis in Timed Circuits</i> , Electrical Engineering Department – University of Utah, pp. 1-4, Salt Lake City, Utah				
Examiner Signature					Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.